AMENDMENT TO THE CLAIMS

The following claim listing replaces all prior listings and versions of the claims:

LISTING OF CLAIMS

1. (Currently Amended) A mixer circuit, comprising:

a mixer including an IF signal output load portion, an LO signal processing portion, and an RF signal processing portion, which are connected in cascade connection between a power supply and a ground;

an RF signal supplier for supplying an RF signal to the RF signal processing portion;

an LO signal supplier for supplying an LO signal to the LO signal processing portion; and

at least [[a]] one bypass current supply portion for bypassing a bias current of the LO signal processing portion, the at least one bypassing current supply portion including a bypass current source,

wherein the bypass current supply portion additionally supplies a bias current only to the RF signal processing portion.

2. (Cancelled)

3. (Currently Amended) [[A]] The mixer circuit as defined in Claim 1, wherein the mixer is constituted by MOS transistors. ~~where the bypass current supply portion additionally supplies a bias current only to the RF signal processing portion.~~

4. (Cancelled)

5. (Currently Amended) A mixer circuit comprising:

a single balanced mixer including an IF signal output load portion, an LO signal processing portion, and an RF signal processing portion, which are connected in cascade connection between a supply voltage and a ground;

an RF signal supplier for supplying an RF signal to the RF signal processing portion;

an LO signal supplier for supplying an LO signal to the LO signal processing portion;

at least one bypass current supply portion for bypassing a bias current of the LO signal processing portion, the at least one bypass current supply portion including a bypass current source, wherein the bypass current supply portion includes a first bypass current source for additionally supplying a bias current only to an RF transistor, which is connected between the power supply and a drain terminal of the RF transistor; [[and]]

said IF signal output load portion including a first load resistor having an end connected to the power supply and another end connected to a first IF output terminal, and a second load resistor having an end connected to the power supply and another end connected to a second IF output terminal;

the RF signal processing portion including an RF transistor having a source terminal connected to the ground;

said LO signal processing portion including a first LO transistor having a source terminal connected to a drain terminal of the RF transistor and a drain terminal connected to the first IF output terminal, and a second LO transistor having a source terminal connected to the drain terminal of the RF transistor and a drain terminal connected to the second IF output terminal.

6. (Cancelled)

7. (Currently Amended) [[A]] The mixer circuit as defined in Claim 5, wherein the single balanced mixer is constituted by MOS transistors. ~~where the bypass current supply portion includes a first bypass current source for additionally supplying a bias current only to the RF transistor, which is connected between the power supply and the drain terminal of the RF transistor.~~

8-22. (Cancelled)